CADSTAR

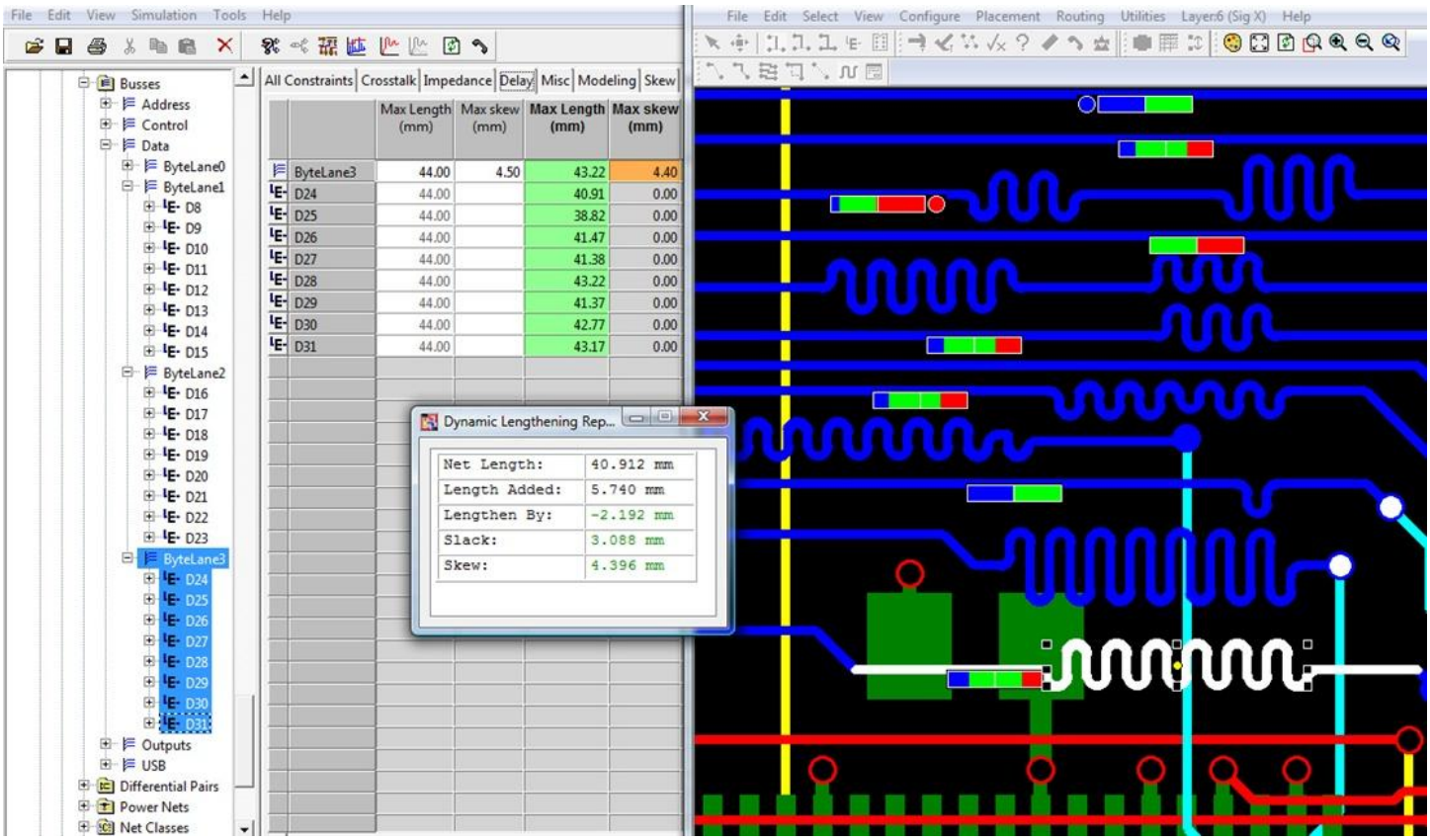
Powerful PCB Design

CADSTAR for High-Speed Design Specialists

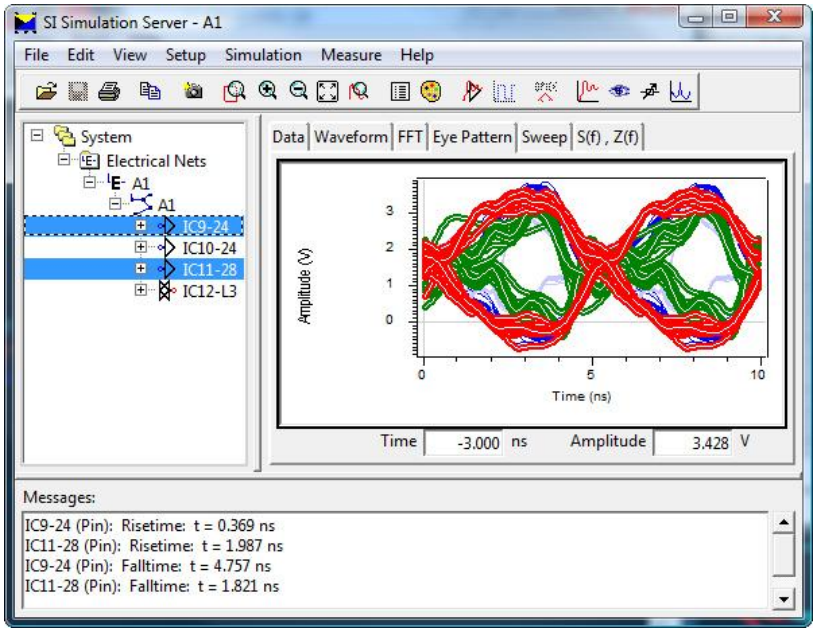
Why is high-speed important?

To meet the growing demand for smaller, faster, more powerful products, IC vendors deliver complex devices that require special consideration of track length, skew, impedance, noise immunity and signal integrity. Implementing these devices in your products requires an increasing knowledge of constraint-driven high-speed design techniques and an in-depth understanding of the science and technology of signal propagation.

The CADSTAR high-speed design tools have been designed to address this challenge, offering you an integrated design environment where constraint entry, verification, analysis and simulation can be performed in one environment.



Constraint management



Central to this technology is the Constraint Manager, a powerful constraint entry and analysis tool that is instantly familiar to engineers as it uses the industry standard spreadsheet interface. The designer can enter either length or delay-based constraints, and net topologies can be determined automatically from the device models specified in the CADSTAR library. You can instantly review the results of these changes on the signal integrity of the design and then make informed choices on the best approach to avoid problems.

Based on your PCB layout, Constraint Manager can automatically allocate nets into various item types including power, busses and differential pairs. Groups of nets, such as a data bus or byte lane, can then be assigned a collective constraint such as a skew or maximum length.

Routing options

The CADSTAR Place and Route Editor high-speed routing tools accommodate all constraints, yet allow designers the flexibility to temporarily override DRC rules, choose how to display constraint markers, whether push-aside and auto-cleanup are required, and a host of other options.

Depending on the complexity of the design and the types of devices used, you can switch to delay-based rules where the router uses IBIS device models and a field solver solution to provide an accurate calculation of impedance and timing characteristics.

Exploration

It is possible to explore signal integrity with CADSTAR Signal Integrity Verify at the conceptual level, even before the net has been routed, to determine termination strategies and the impact of alternate topologies. A range of scenarios can be explored and saved for later review, including analysis of swept design parameters and generation of eye diagrams.

Once the nets have been routed the designer can run an in-place simulation simply by selection of the net within the routing environment, saving time and ensuring the focus remains on the current design elements.

Power plane analysis

As the number of power rails increases and their values continue to decrease, the ability of planes within a design to distribute power to the correct devices can be seriously degraded by both the physical definition of the plane and the distribution of decoupling. CADSTAR Power Integrity Advance helps you determine the level of risk to your PCB and through analysis of the planes, guides you to resolve power distribution problems.