CADSTAR

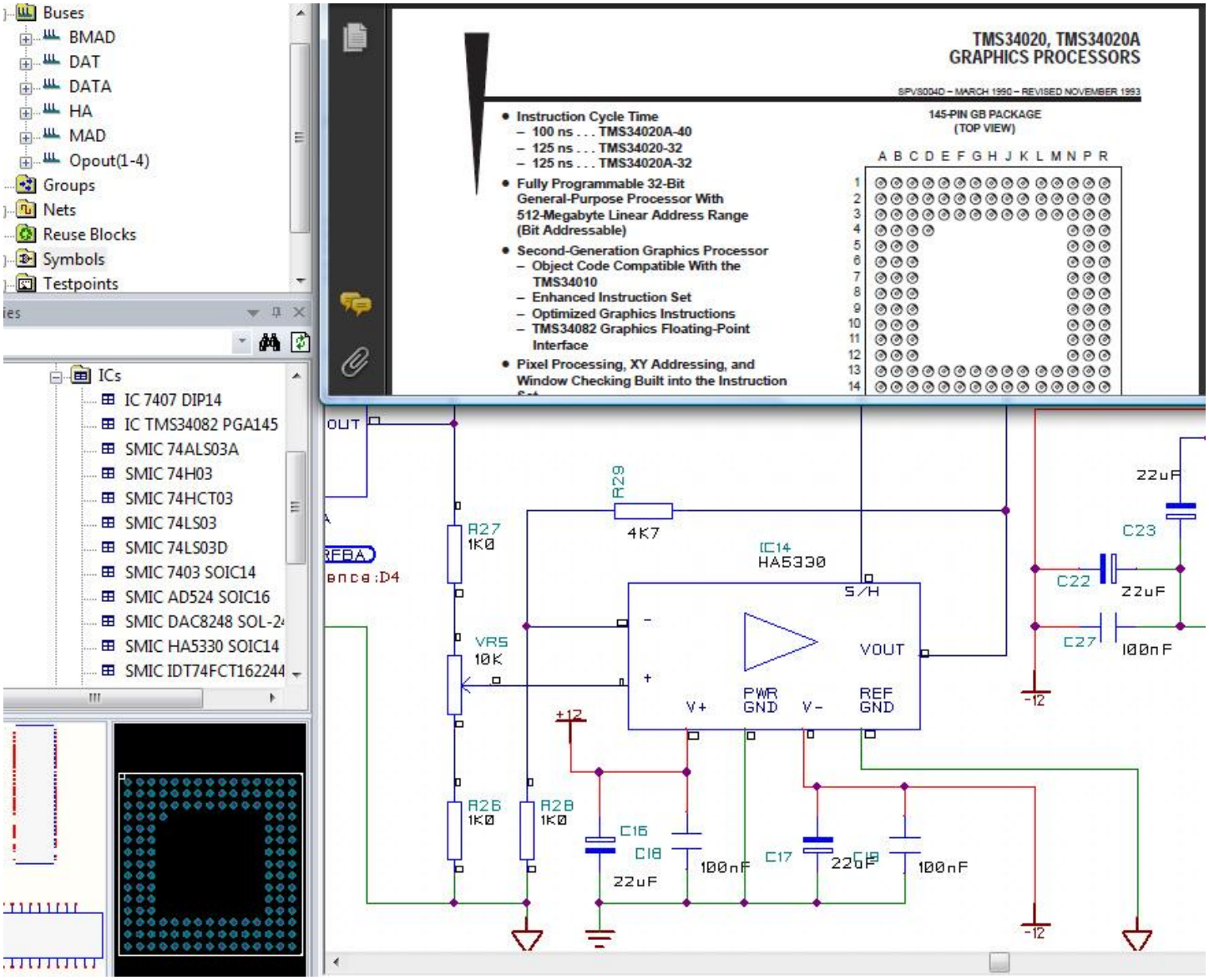
Powerful PCB Design

CADSTAR for Electronic Design Engineers

Innovation

Your PCB design challenges require innovative solutions, so being able to capture your ideas in a fast, effective, error-free manner is critical. CADSTAR Schematic Capture provides you with a flexible, yet powerful, design platform that includes:

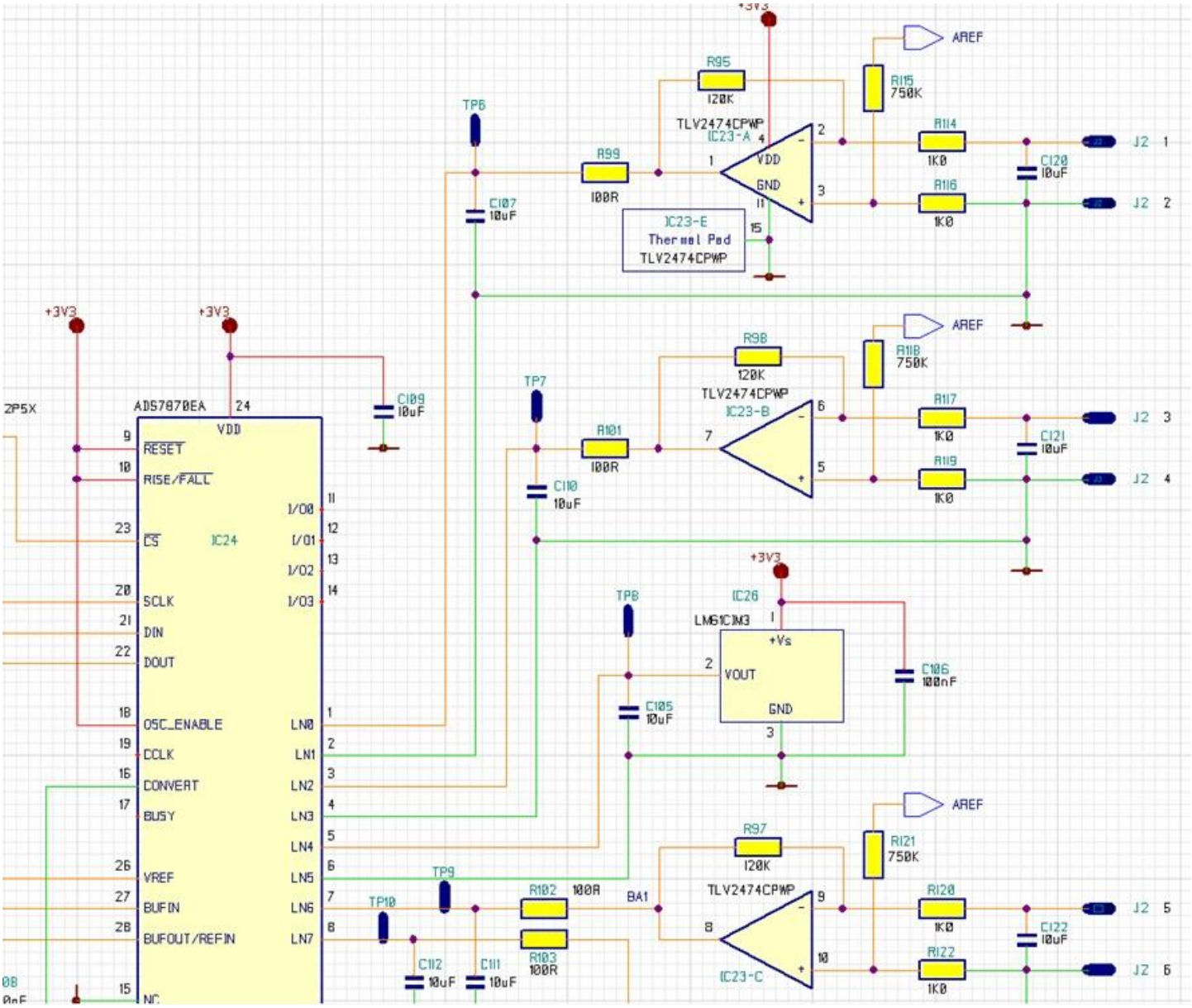
- A choice of design methodology that lets you design at the symbol, part, block or sheet level with a multi-layer hierarchical or multi-sheet design environment.
- An intelligent, connective database that accurately captures design intent and maintains design integrity throughout the CADSTAR flow.
- A fully customizable design environment with the same GUI in Schematic, PCB Layout, Library Editor and Routing environments.
- A range of supporting tools to help you define, simulate and manage your design data


Buses
BMAD
DAT
DATA
HA
MAD
Opout(1-4)
Groups
Nets
Reuse Blocks
Symbols
Testpoints
ICs
IC 7407 DIP14
IC TMS34082 PGA145
SMIC 74ALS03A
SMIC 74H03
SMIC 74HCT03
SMIC 74LS03
SMIC 74LS03D
SMIC 7403 SOIC14
SMIC AD524 SOIC16
SMIC DAC8248 SOL-24
SMIC HA5330 SOIC14
SMIC IDT74FCT162244
TMS34020, TMS34020A
GRAPHICS PROCESSORS
SPVS004D – MARCH 1990 – REVISED NOVEMBER 1993
Instruction Cycle Time
– 100 ns . . . TMS34020A-40
– 125 ns . . . TMS34020-32
– 125 ns . . . TMS34020A-32
Fully Programmable 32-Bit General-Purpose Processor With 512-Megabyte Linear Address Range (Bit Addressable)
Second-Generation Graphics Processor
– Object Code Compatible With the TMS34010
– Enhanced Instruction Set
– Optimized Graphics Instructions
– TMS34082 Graphics Floating-Point Interface
Pixel Processing, XY Addressing, and Window Checking Built into the Instruction
145-PIN GB PACKAGE
(TOP VIEW)
A B C D E F G H J K L M N P R
OUT
R29
4K7
R27
1KØ
IC14
HA5330
S/H
VR5
10K
VOUT
V+
PWR GND
V-
REF GND
+12
-12
R26
1KØ
R28
1KØ
C16
C18
22uF
100nF
C17
22uF
C19
100nF
C22
22uF
C23
22uF
C27
100nF

Library management

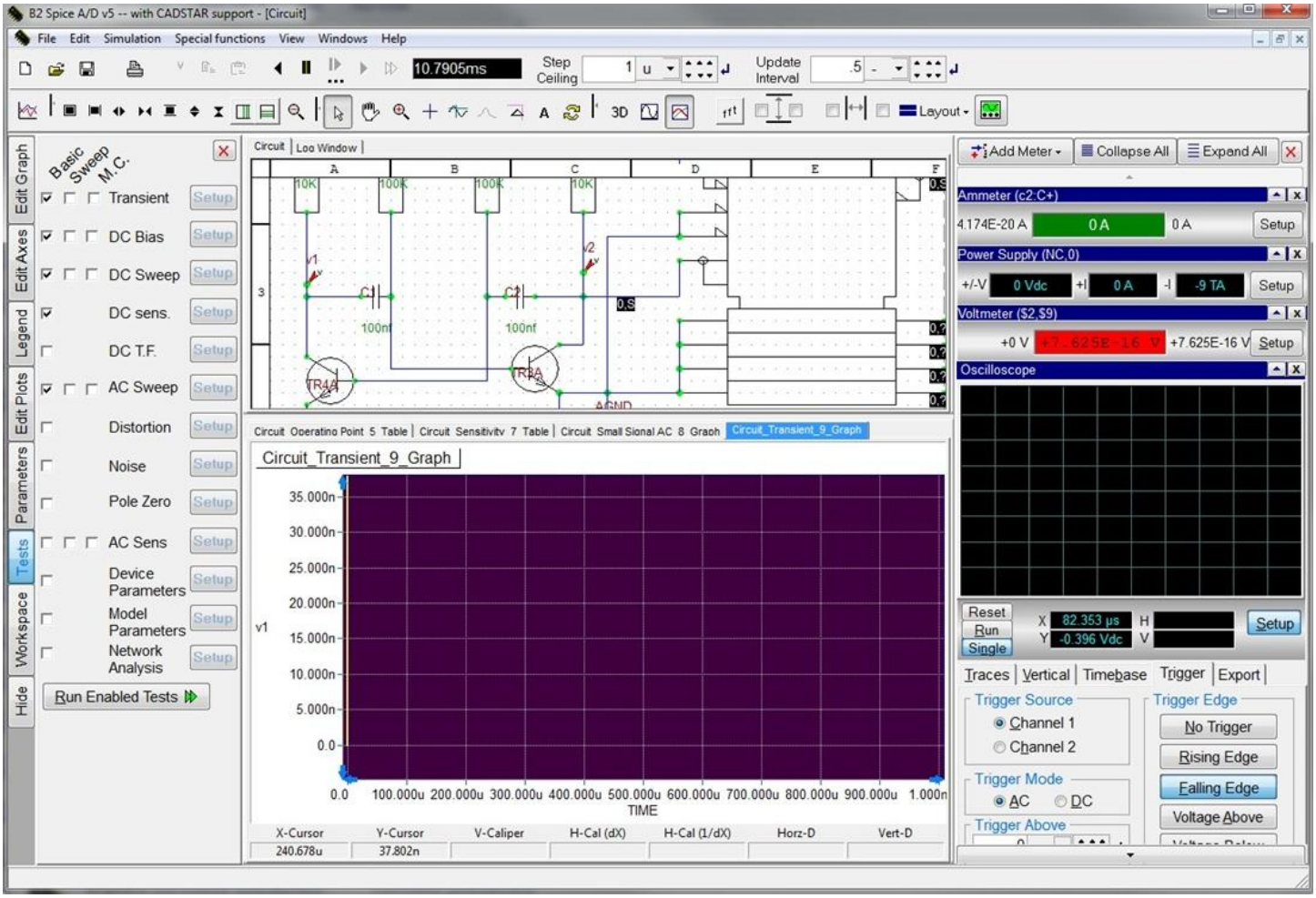
Libraries are key to the design process, so Zuken gets you ahead of the game with an on-line library of more than 250,000 parts from leading vendors such as Actel, Analog Devices, Intel, Texas and Zetex. Dynamic links can be added to a supplier's datasheet or website so engineers have the latest information at their fingertips.

If you need to integrate CAD data with your engineering database, CADSTAR supports access to any ODBC-compliant data source, enabling links to the latest corporate information as well as the ability to run parametric searches to locate the correct part using a range of attributes.



Repeatability

Need to include repeated or pre-defined 'golden circuit' design blocks? Create them as reuse blocks and build your own library toshare with colleagues. Reuse blocks in schematics can automatically link to prerouted blocks in PCB layout, including placement, routing, copper and text to help you save time and enhance quality during layout and test.



FPGA integration

A growing number of designs include programmable devices that let you extend and customize the functionality of your products. Today's high capacity devices have high pin counts that make symbol definition and management of pin connectivity increasingly complex; not just in the Schematic but throughout the design process.

CADSTAR FPGA, founded on industry-leading technology from Aldec Inc, enables FPGA development, synthesis and verification using a vendor-independent, intuitive design methodology. Single-click transfer of pin information to and from CADSTAR allows fast, efficient creation of functional block symbols and synchronization of pin changes to optimize the routability and performance of the design.

- Download our free 30 day CADSTAR FPGA evaluation

Simulation

CADSTAR supports tools for analog, digital and mixed mode simulation. You can export a Spice netlist for simulation.

Variant management

Variant Manager allows you to define market-specific products that broaden the scope and appeal of your range, improve cost control and enhance product differentiation. CADSTAR allows you to create, view and list multiple design variants by excluding selected items or specifying alternate parts.

Constraint-driven design

Even the most straightforward modern processor and memory combinations uses a DDR interface, so it makes sense to add the critical pin, net and timing constraints directly into the logical circuit design. The CADSTAR Constraint Browser is the ideal environment for entering and managing even the most complex rules, using a familiar spreadsheet style interface that helps capture and document design intent.

Placement planner

Correct placement of design blocks, or even individual components, is increasingly important as noise margins are reduced and switching speeds increase. CADSTAR Placement Planner offers a full suite of placement and board setup utilities (e.g. layer stackup, design rules, etc.) to provide the design engineers with the tools to define critical placement.